Amitabh **Yadav**

PH.D. CANDIDATE, DIGITAL/MIXED-SIGNAL IC DESIGN ENGINEER

IEEE Student Member | D.O.B. March 27, 1995 | Nationality: INDIAN | Current Residence: Geneva, Switzerland

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Summary

I'm a PhD student specializing in ultra-low-power ASIC design at EPFL - a cheerful nerd who loves Vim, Linux, Mathematics, Physics and Problem solving. I'm 3+ years experienced in designing complex computing systems in Experimental Physics, Space systems and safety critical electronics in my prior roles at EPFL, CERN and Berkeley National Lab. Briefly, I have also worked on topics in theoretical CS of pattern matching algorithms in High-Energy Physics.

My interests are ***Brain-Computer Interfaces****,* ***Computing In-Memory****,* ***Computer Architecture*** *&* ***Hardware/Software Co-design****.*

Education

EPFL (École Polytechnique Fédérale de Lausanne)

Lausanne, Switzerland

DOCTOR OF PHILOSOPHY (SPL. DIGITAL & MIXED-SIGNAL IC DESIGN) *March 2024 - present*

- Designing feature extraction, digital signal processing, and machine learning ASICs used in neural implants for diagnosis and treatment of neurological disorders.
- Verification and Testing through simulations, as well as electrical and biological (in-vitro and in-vivo) experiments.
- Teaching: NX-422 Neural Interfaces, EE-330 Digital IC Design

UC Berkeley (University of California, Berkeley)

Berkeley, USA

RESEARCH AFFILIATE (HEP.QPR) *November 2019 - September 2021*

- Courses: CS61C Machine Structures, EECS151 Digital Design and Integrated Circuits, EECS252 Advanced Computer Architecture, EECS290-2 Hardware for Machine Learning.

TU Delft (Delft University of Technology)

Delft, Netherlands

M.SC. COMPUTER ENGINEERING (SPL. QUANTUM COMPUTING) (OVERALL GPA: 8.2/10.0) *September 2017 - August 2019*

- Master Thesis: **'Micro-architecture Design for control of Spin Qubit Quantum Processor'**. Thesis Grade: 9/10. (1 year)
- Teaching Assistant: (i) 'The Building Blocks of a Quantum Computer: Part 1 and Part 2' MOOC on edx.org (12+ weeks); (ii) 'EE1D11 Digital Systems A: Programming in C' Undergraduate Course. (8 weeks)
- 'Quantum Information Theory' at **DPHYS, ETH Zurich**
- 'Quantum Computing for High Energy Physics' meet (November 2018) at **CERN, Geneva**.

UPES (University of Petroleum and Energy Studies)

Dehradun, India

B.TECH. ELECTRONICS ENGINEERING (OVERALL GPA: 3.1/4.0) *August 2013 - June 2017*

- Final Project: **'Design & Simulation of 16-bit microcontroller'**. Thesis Grade: 4/4. (8 months)
- Research Assistant at Embedded Systems Lab, UPES

Experience

EPFL (École Polytechnique Fédérale de Lausanne)

Lausanne, Switzerland

VISITING RESEARCHER (DIGITAL IC DESIGN ENGINEER) *July 2023 - February 2024*

- Implemented feature extraction and classification kernel as ASIC for seizure detection.
- Developed ZynqMPSoC testbench for real-time streaming data for Neural Decoder IC for brain-machine interfaces. [News1]

CERN (Conseil Européen pour la Recherche Nucléaire)

Geneva, Switzerland

RESEARCH FELLOW (SOC/FPGA DIGITAL DESIGN AND ELECTRONICS) *November 2020 - April 2023*

- Digital Design, verification and embedded software development for CERN's safety-critical (SIL2) Radiation Monitoring Electronics devices running on **Zynq MPSoCs**.
- Developed the continuous integration and continuous delivery (CI/CD) implementation for hardware projects comprising of automated test, build and automated embedded linux build.
- Developed the TCP/IP C networking library, ROMULUSlib (published) and a FPGA-Linux Cosimulation framework using QEMU.
- CERN official visits guide for SM-18 LHC Electromagnet Test facility, Anti-matter Factory and ATLAS Underground experiment

LBNL (Lawrence Berkeley National Laboratory)

Berkeley, California, U.S.A.

Research Associate, Physics Division — *November 2019 - October 2020*

- Developed **Quantum Hough Transform** algorithm using HHL, Quantum Phase Estimation and Grovers-Long Algorithm for ATLAS/CERN Track Reconstruction. [**Machine Learning for Fundamental Physics Group**] [News1] [News2]
- Developed an early prototype of Quantum Pattern Recognition algorithm for particle tracking for the ATLAS Detector.

QuTech/TU Delft

Delft, Netherlands

Research Assistant, Quantum & Computer Engineering Lab — *August 2018 - September 2019*

- Developed the **CC Spin Micro-architecture Design** targeting high qubit count control for Spin Qubit Quantum Processor.
- Implemented the design on a Cyclone-V SoC-FPGA dedicated for translating the Instruction Set (QISA) to sequences of arbitrary I/Q and DC Pulses. The micro-architecture is interfaced with a FPGA controlled Direct Digital Synthesis (DDS) h/w communicating via high-speed LVDS signals for multi-channel synchronous waveform generation. It comprises of a Quantum Pipeline, a Microcode Unit, Timing Control Unit and SPI Master (DDS controller) to perform Qubit operations.

DARE (Delft Aerospace Rocket Engineering)

Delft, Netherlands

Electronics Integration & Test Engineer — *October 2017 - July 2018*

- Stratos-III Sounding Rocket Avionics: **ADC-DAQ Firmware Development** on ARM Cortex-M3; PCB Design on Altium Designer.
- Assisted the Propulsion Team in Manufacturing Sorbital, Paraffin & Aluminum based Solid Rocket Fuel
- PCB Design using Altium Designer 18

CERN (Conseil Européen pour la Recherche Nucléaire)

Geneva, Switzerland

Summer Student (ATLAS Pixel Group, EP-ADE-ID) — *June 2017 - August 2017*

- Developed a **front-end DAQ firmware for ATLAS Inner Detector's FEI-4 Silicon Pixel Chip** on Xilinx Kintex KC705.
- Integrated the IPBus (UDP/IP) protocol (front-end monitoring) and 8b/10b encoded Rx/Tx Core to communicate with back-end Gigabit Transceiver (GBT) protocol. Further, developed a data_routing entity called 'E_Link Bank'. (**Report**) [News]

BARC (Bhabha Atomic Research Center)

Mumbai, India

Project Trainee (Data Acquisition & Processing Systems (DA&PS) Group) — *June 2016 - August 2016*

- Developed **Compression and De-Noising library** for A, B and C Scan Ultrasonic Scan Data for application in NDT of Materials.
- Achieved loss-less data compression up to 75.37% in C-Scan data using standard information coding algorithms.
- Analyzed compression ratios & noise in Lossy compression algorithms including 1-D & 2-D DCT, DFT and Wavelet Transform.

Technical Skills

Programming C (Expert), C++ (Moderate), VHDL, SV and Verilog (Expert), Tcl, Shell, GNU Make/Autotools, Python/PyTorch.

CS Frameworks Docker, Kubernetes, RISC-V, Gemmini/RocketChip, Git CI/CD, Javascript, NodeJS, PostgreSQL.

Software Tools MATLAB, PCB design using Altium Designer, Xilinx Vivado/Vitis, Petalinux, QuestaSim, Cadence Genus, Virtuoso and Innovus, Synopsys Fusion Compiler, LaTeX, Anaconda, IBM-QISKIT.

Academic Projects

- Running **Shor's Algorithm on IBM Quantum Experience** using IBM-Q QISKit. [Report]
- **BICMOS5 Fabrication & Measurement** of IC parameters in Else Kooi IC fabrication Cleanroom, TU Delft.
- OpenCL implementation of Smith-Waterman Algorithm for **Protein/DNA Sequencing**.
- Performance improvement of **Plasma processor core (opencores.org)** in VHDL. (Processor Design Project)
- **Parallel Poisson Solver** on Distributed Memory HPC cluster using MPI. (High Performance Computing)
- Design and Jitter Analysis of **Quadrature Phase By-6 frequency divider** in Cadence Spectre. (Digital IC Design)
- Development of Classic Snake Game using **Software Design Patterns in Java**. [ATHENS Programme 2017]
- Modelling and Simulation of a **16-bit Microcontroller in Xilinx/VHDL**. [Bachelors Thesis Project]
- Embedded Hardware development of AVR-MCU based **Audio-Signal Morse Code Encoding/Decoding**.
- **Wireless Sensor Network** system for: (i) Landslide Forecasting (2017) and, (ii)Patient Monitoring and Tracking System(2015). Funded research projects (INR 45,000) [UPES Best Research Award 2017]

National & International Competitions

Lockheed Martin Roll-On/Roll-Off Design Challenge — *New Delhi*

Electronics Engineer (Phase II) — *August 2015 - May 2017*

- Developed the detailed technical design of Aerial Surveillance System, Payload Control and Communication System.
- **Excelled with National Rank 1** in the Critical Design Phase (Phase-II).
- Secured a research grant by the Aerospace and Defense giant, **Lockheed Martin** (USD 25,000 + USD 40,000) to manufacture the prototype payload structure for C-130J Super Hercules Military Aircraft. [News1] [News2]

Intercollegiate Rocket Engineering Competition (IREC) 2017 — *Spaceport America, U.S.A.*

Avionics and Payload Engineer — *August 2016 - May 2017*

- Developed the **avionics and telemetry systems** in the **Sounding Rocket 'Kalam'** for Team Garud (Rocketry Division of UPES).
- Lead the development of a Cansat payload performing stable decent using triple-modular redundancy electronics.
- 'Kalam' is a 2.8 meters tall Solid COTS-propellant based rocket capable of carrying scientific payloads weighing up to 4 kg.

Cansat Competition 2015, '16 & '17 — *Texas, U.S.A.*

Technical Advisor 2017, Team Leader (Electronics) 2016, Team Member 2015 — *August 2015 - June 2017*

- **International Rank 1** (2017) and **4** (2016). Various roles in development & integration of Sensor Subsystem, Telemetry System, Recovery System, real-time decent monitoring system, and Ground Control Station for rocket payload. [News1] [News2]

Certifications

- 'Mixed-Signal Circuit Design', 'ASIC Design for 5nm era' by **MEAD, EPFL** (September 2024, April 2025).
- 'Advanced Digital IC Design and Implementation' by **UKRI Europractice/EPFL** (November, 2023).
- 'Comprehensive Digital IC Design' by **UKRI Europractice/CERN** (April, 2023).
- 'Hardware-Efficient Machine Learning across the Circuit-Architecture-Scheduling Stack' (Nov 2022) at **IMEC, Belgium**.
- Nature conference on **Technologies for Neuroscience** (Online)
- 'The Quantum Wave in Computing' (Jan - May, 2020) at **Simons Institute for the Theory of Computing, UC Berkeley**.
- 'BigCompute20' Conference held Feb 11 - Feb 12, 2020, organized by **Rescale Inc. in San Francisco**.
- "Venture Lab: Business Creation ENGINEERING" workshop (1 week) in **EPFL Lausanne, Switzerland**.
- 'Quantum Information for Developers 2018' Summer School at **Institute for Theoretical Physics, ETH Zurich**.
- 'Quantum Computing for High Energy Physics' meet (November 2018) at **CERN, Geneva**.
- 'TUD15 Software Design Patterns' 2018 at **ATHENS Programme**
- Embedded Design & Technology Workshop 2016 by Prof. D.V. Gadre. (**Texas Instruments Lab, NSIT Delhi**)
- Network Security and Ethical Hacking Workshop 2015 (**Nettech Pvt. Ltd.**)
- Class Representative (4 years), Placement Coordinator (1 year) and University DSA/Discipline Committee Head (1 year).
- Cross Country Cycling - Around Lac Leman (185km), Vlaadingen to Delft (115 km) etc.

Industry: Expert VHDL (Doulos, London) - 2021; Embedded Linux (Doulos, London) - 2021;
High Voltage Engineering, First-Aid, Saving Life Actions (CERN) - 2022;
Cadence Static Timing Analysis (2022); Cadence RTL-to-GDSII Flow (2022);

MOOCs: Particle Physics: An Introduction (University of Geneva, Coursera) - 2017;
Quantum Cryptography (TU Delft & Caltech, EDX) - 2018;
Quantum Machine Learning (University of Toronto, EDX) - 2019;

Publications

- D. Alex, **A. Yadav**, J. Joo et al., "A 32-Channel 196-μW Logarithmic SoC for Brain Network Connectivity Extraction and Adaptive Psychiatric Symptom Classification ," in Symposium on VLSI Technology and Circuits (VLSI Symposium), Kyoto, Japan, pp. 1-3 (2025).
- M. Shaeri, U. Shin, **A. Yadav**, R. Caramellino, G. Rainer and M. Shoaran, "A 2.46-mm2 Miniaturized Brain-Machine Interface (MiBMI) Enabling 31-Class Brain-to-Text Decoding ," in IEEE Journal of Solid-State Circuits (JSSC), vol. 59, no. 11, pp. 3566-3579, Nov. 2024.
- M. Shaeri, U. Shin, **A. Yadav** et al. "MiBMI: A 192/512-Channel 2.46mm2 Miniaturized Brain-Machine Interface Chipset Enabling 31-Class Brain-to-Text Conversion through Distinctive Neural Codes " (IEEE ISSCC 2024).
- **A. Yadav**, H. Boukabasche, N. Gerber, K. Ceesay-Seitz, D. Perrin, "ROMULUSlib: An autonomous, TCP/IP-based, multi-architecture C networking library for D.A.Q. and Control applications ", International Conference on Accelerator and Large Experimental Physics Control Systems (ICALEPCS) Conference, Shanghai Advanced Research Institute, China (October 2021).
- H. Gray, J. Wonho, V. R. Pascuzzi, R. Sawada, K. Terashi, **A. Yadav** "Quantum Pattern Recognition for Tracking in High Energy Physics ", SnowMass 2021.
- **Amitabh Yadav**, Nader Khammassi, Koen Bertels, *"CC-Spin: A scalable Microarchitecture design for Control of Spin-Qubit Quantum Accelerator"* Preprint. (2020).
- K. Bertels, A. Sarkar, T. Hubregtsen, M. Serrao, A. A. Mouedenne, **A. Yadav**, A. Krol, I. Ashraf "Quantum Computer Architecture Toward Full-Stack Quantum Accelerators ," in IEEE Transactions on Quantum Engineering, vol. 1, pp. 1-17, 2020, doi: 10.1109/TQE.2020.2981074.
- **A. Yadav** et al. "Wireless Sensor Network Based Patient Health Monitoring and Tracking System", in Proceeding of International Conference on Intelligent Communication, Control and Devices, p. 903-917, Springer (2017)

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